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PTO/SB/06A (10-96)

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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Complete if Known

Application Number	09/438,856
Filing Date	November 12, 1999
First Named Inventor	
Group Art Unit	2763
Examiner Name	
Attorney Docket Number	3104P002

Sheet 1 of 3

U.S. PATENT DOCUMENTS

Exam. Initials	Cite No.	Document Number	Date	Name	Class	Sub-class	Filing Date (if appropriate)
E6	A	4,656,603	04/07/87	Dunn			
	B	4,675,832	06/23/87	Robinson et al.			
	C	4,813,013	03/14/89	Dunn			
	D	4,829,446	05/09/89	Draney			
	E	4,878,179	10/31/89	Larsen et al.			
	F	4,965,741	10/23/90	Winchell et al.			
	G	5,019,992	05/28/91	Brown et al.			
	H	5,111,413	05/05/92	Lazansky et al.			
	I	5,164,911	11/17/92	Juran et al.			
	J	5,278,769	01/11/94	Bair et al.			
	K	5,325,309	06/28/94	Halaviati et al.			
	L	5,463,563	10/31/95	Bair et al.			
	M	5,471,399	11/28/95	Tanaka et al.			
	N	5,544,067	08/06/96	Rostoker et al.			
	O	5,623,418	04/22/97	Rostoker et al.			
	P	5,629,857	05/13/97	Brennan			
	Q	5,271,959	02/24/98	Nakamura et al.			
	R	5,787,268	07/28/98	Sugiyama et al.			
	S	5,801,958	09/01/98	Dangelo et al.			
	T	5,889,677	03/30/99	Yasuda et al.			

FOREIGN PATENT DOCUMENTS

Exam. Initials	Cite No.	Document Number	Date	Country	Class	Sub-class	Translation Yes	No

Examiner Signature

GARCIA-OTERO

Date

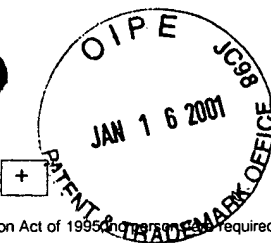
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10/19/02

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				Examiner Name	
Sheet	2	of	3	Attorney Docket Number	3104P002

OTHER ART (Including Title, Author, Date, Pertinent Pages, etc.)

Exam. Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
EG	U	GOODALL, S. Analog/Mixed Signal Fault Diagnosis Algorithm and Tool Review, AutoTestCon Proceedings 1994,m 351-359, USA
EG	V	SIMPSON, W.R. AND SHEPPARD, J.W., Fault Isolation in an Integrated Diagnostic Environment. IEEE Design & Test, March 1993, 52-66, Vol. 10, No. 1, USA
EG	W	PAN, C.Y. AND CHENG, K.T., Test Generation For Linear, Time Invariant Analog Circuits 3rd IEEE Intl. Mixed-Signal Testing Workshop, June 3-6, 1997, 93-100, USA 98-100 EG
EG	X	DILL, H., A Comparison of Conventional and Inference Model Based TPS Development Processes, AutoTestCon, 1995, 160-168, USA
EG	Y	DILL, H., BRATTON, K., SPARR, C., AND PITZEN, L., Application of Analog & Mixed Signal Simulation Techniques to the Synthesis and Sequencing of Diagnostic Tests.
EG	Z	UL Standards-On-Diskette User Guide, Underwriters Laboratories, Inc., ISBN 0-7629-0093-8, 1996, 17, USA
	AA	CASS Red Team Package data item DI-ATTS-80285B, Fig. 1-SRA/SRU Fault Accountability Matrix Table, 11
EG	AB	NAGEL, L.W. AND PEDERSON, DO. Spice 2: A Computer Program to Simulate Semiconductor Circuits, ERL Memo No. ERL-M520, University of California, Berkeley, May 9, 1975 EG.
EG	AC	JOHNSON, B., QUARLES, T., NEWTON, AR., PDEERSON, DO., SANGIOVANNI-VINCENTELLI, A. Spice 3 Version 3f User's Manual, University of CA, BERKELEY OCT 1992
EG	AD	IsSpice4 User's Guide, Intusoft, 1997, USA ONLY 3 PAGES SUBMITTED (BIBLIOGRAPHIC DATA) EG.
EG	AE	COX., F., KUHN, W., MURRAY, J., AND TYNOR, S., Code-Level Modeling in XSPICE, Proceedings of the 1992 Intl. Symp. of Circuits and Systems, May 1992, USA
EG	AF	XSPICE User's Manual, Georgis Institute of Research, Georgia Institute of Technology, 1992, USA
EG	AG	HAMIDA, NB., SAAB, K., MARCHE, D., KAMINSKA, B., AND QUESNEL, G., LIMSoft: Automated Tool for Design and Test Integration of Analog Circuits, 2nd IEEE International
	AH	HAMIDA, NB., AND KAMINSKA, B., Analog Circuit Fault Diagnosis-Based-on-Sensitivity Computation and Functional Testing, IEEE Design and Test of Computers, 1992, 30-39

Examiner Signature	GARCIA-OTERO	Date Considered	10/19/02
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